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S/N Unknown

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Dustin P. Wood

Examiner: Unknown

Serial No.: Unknown

Group Art Unit: Unknown

Filed: Herewith

Docket: 884.159US2

Title: CHIP PACKAGE WITH DEGASSING HOLES

PATENT

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

Before taking up the above-identified application for examination, please enter the following amendments.

IN THE SPECIFICATION

On page 1, after the title, please add the following paragraph: -- This application is a Continuation of U.S. Application No. 09/388,768 filed September 2, 1999. --

IN THE CLAIMS

Please cancel claims 1-29 and add the following new claims.

Ad contd

30. An integrated circuit package comprising:
a first conductive layer having a first grid of holes;
a second conductive layer parallel to the first conductive layer, the second conductive layer having a second grid of holes offset from the first grid of holes; and
a dielectric layer between the first and second conductive layers.

31. The integrated circuit package of claim 30 further comprising a signal layer embedded in the dielectric layer.

32. The integrated circuit package of claim 31 wherein the signal layer includes at least one signal trace.

33. The integrated circuit package of claim 32 wherein the at least one signal trace includes segments that are parallel and substantially 45 degrees to each other.

*Ad
Contd*

34. The integrated circuit package of claim 32 wherein the first and second grids of holes have an x direction and a y direction, neither of which being parallel to the at least one signal trace.

35. The integrated circuit package of claim 34 wherein the at least one signal trace includes at least one segment rotated substantially 22.5 degrees relative to the x direction.

36. The integrated circuit package of claim 30 wherein the first grid of holes includes holes spaced with equal pitch in an x direction and in a y direction.

37. The integrated circuit package of claim 30 wherein the first grid of holes includes holes spaced with non-equal pitch in an x direction and in a y direction.

38. The integrated circuit package of claim 37 further comprising signal traces within the dielectric layer, the signal traces being at angles other than 0, 45, and 90 degrees relative to the first and second grids of holes.

39. An integrated circuit package comprising:
a core having first and second sides; and
built-up layers on the first side of the core, the built-up layers including first and second conductive layers with non-aligned grids of degassing holes.

40. The integrated circuit package of claim 39 further comprising a signal layer between the first and second conductive layers, the signal layer including at least one signal trace with segments rotated relative to the grids of degassing holes.

41. The integrated circuit package of claim 39 further comprising built-up layers on the second side of the core, the built-up layers on the second side of the core including third and fourth conductive layers with non-aligned grids of degassing holes.

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Count 42. The integrated circuit package of claim 39 wherein:

the first conductive layer includes a first grid of degassing holes arranged in an x direction and a y direction; and

the second conductive layer includes a grid of degassing holes offset from the first grid of degassing holes in at least one of the x direction and the y direction.

43. The integrated circuit package of claim 39 wherein:

the first conductive layer includes a first grid of degassing holes arranged in an x direction and a y direction; and

the second conductive layer includes a grid of degassing holes offset from the first grid of degassing holes in both the x direction and the y direction.

44. The integrated circuit package of claim 43 further comprising:

a signal layer between the first and second conductive layers, the signal layer including at least one trace segment rotated substantially 22.5 degrees relative to the x direction.

45. The integrated circuit package of claim 44 further comprising built-up layers on the second side of the core, the built-up layers on the second side of the core including third and fourth conductive layers with non-aligned grids of degassing holes.

46. The integrated circuit package of claim 45 wherein:

the third conductive layer includes a first grid of degassing holes arranged in the x direction and the y direction; and

the fourth conductive layer includes a grid of degassing holes offset from the third grid of degassing holes in both the x direction and the y direction.

47. The integrated circuit package of claim 46 further comprising:

a signal layer between the third and fourth conductive layers, the signal layer including at least one trace segment rotated substantially 22.5 degrees relative to the x direction.

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48. A method of manufacturing built-up layers on a core comprising:
depositing a first metal layer with a first grid of holes on a first side of the core;
depositing a first dielectric layer on the first metal layer;
depositing a first signal layer on the first dielectric layer;
etching the first signal layer to produce at least one signal trace;
depositing a second dielectric layer on the first dielectric layer and the at least one signal trace; and

depositing a second metal layer with a second grid of holes on the second dielectric layer, such that the second grid of holes does not align with the first grid of holes.

49. The method of claim 48 wherein etching comprises:

etching the first signal layer to produce at least one signal trace including segments parallel and 45 degrees to each other.

50. The method of claim 49 wherein the first grid of holes includes holes in an x direction and a y direction, and wherein etching comprises:

etching the first signal layer to produce at least one signal trace including segments that are not parallel to either the x direction or the y direction.

51. The method of claim 48 wherein the first grid of holes includes holes in an x direction and a y direction, and wherein etching comprises:

etching the first signal layer to produce at least one signal trace segment that is rotated substantially 22.5 degrees relative to the x direction.

52. The method of claim 51 wherein depositing a second metal layer comprises:
depositing the second metal layer such that the second grid of holes is offset from the first
grid of holes in either the x direction or the y direction.

53. The method of claim 51 wherein depositing a second metal layer comprises:
depositing the second metal layer such that the second grid of holes is offset from the first
grid of holes in both the x direction or the y direction.

54. The method of claim 48 further comprising:

- depositing a third metal layer with a third grid of holes on a second side of the core;
- depositing a third dielectric layer on the third metal layer;
- depositing a second signal layer on the third dielectric layer;
- etching the second signal layer to produce at least one signal trace;
- depositing a fourth dielectric layer on the third dielectric layer and the at least one signal trace; and
- depositing a fourth metal layer with a fourth grid of holes on the fourth dielectric layer, such that the fourth grid of holes does not align with the third grid of holes.

REMARKS

Claims 30-54 are now pending in this application.

CONCLUSION

The Examiner is invited to contact the Applicant's attorney if prosecution of the present application can be assisted thereby.

Respectfully submitted,

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Date of Deposit: March 7, 2001

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